SPECIFICATION

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A SYSTEM AND METHOD FOR CORRECTING TIMING SIGNALS IN INTEGRATED CIRCUITS

Background of the Invention

[0001] Field of the Invention

[0002] This invention relates generally to timing systems for integrated circuits (IC's), and more specifically, to novel circuits for altering the clock speed used to send and receive data within the IC based on physical characteristics of the IC.

[0003] Discussion of the Prior Art

[0004] In current integrated circuit design technology, circuits are typically designed to meet the worst case operating condition and technology process conditions. However, it is the case that typical process and operating conditions are not worst case resulting in existing margins in most worst case paths. If the design can take advantage of the real world margin, then significant performance gain could result.

[0005] It would thus be highly desirable to provide an Integrated Circuit equipped with error correction circuitry for ensuring that data send and receive rates within the IC are maximized.

[0006] It would be further highly desirable to provide an Integrated Circuit equipped with error correction circuitry for ensuring that data send and receive rates within the IC are maximized in accordance with the physical characteristics of the IC.

Brief Summary of the Invention

[0007] It is an object of the present invention to provide circuitry in IC's to ensure

maximum data send and receive rates within an IC.

[0008] It is a further object of the present invention to provide circuitry in IC's for ensuring that data send and receive rates within the IC are maximized in accordance with the physical characteristics and operating conditions of the IC.

[0009] It is another object of the present invention to provide for serial communications transmitters and receivers, a system and methodology for maximizing data send and receive rates within the IC in accordance with the physical characteristics and operating conditions of the IC.

[0010] According to the invention, there is provided at a data receiving port in an Integrated Circuit, a series of clock taps to enable clocking speed choices. At reset, a learning cycle is implemented whereby a series of predefined transmissions or a pseudo random bit stream are generated from a data transmission source. Along with the data, an error code may be included which may range from simple parity to other forms of error correction.

[0011] In a first embodiment, an ECC generator receives data from the transmitter that is clocked at various clock speeds and, outputs the data plus error correction information according to known techniques. Coupled to the ECC generator device is a novel error correcting code (ECC) check circuit device that verifies receipt of correct data transmitted until a failure point is reached. The clock frequency controlling data transmission and receive circuits is then adjusted to a maximum value that avoids the failure point.

[0012] In a second embodiment, a data error check circuit receives a sequence of data signals on error code lines that are generated at the transmitter and clocked at various clock speeds. The data sequence received at the error checker is actually delayed in time and, is compared to the known transmitted data sequence for verifying receipt of correct data transmitted until a failure point is reached. The clock frequency controlling data transmission and receive circuits is then adjusted to a maximum value that avoids the failure point. In this embodiment, wiring tools are implemented during final product development (PD) cycles to tune the load on the error codes lines in such a way that the delay though these wires will be slightly

greater than the data lines to receiver circuits. During the test time, an error detection circuit will monitor to a first fail point, and then pick a click tap of sufficient guard band to guarantee the error free arrival of the data.

[0013] In a third embodiment, a random number generator is generated with any pseudo-random, linearly distributed algorithm known to skilled artisans (such as XORing the bits with themselves). This unique random number is transmitted throughout a data path of a semiconductor CORE circuit comprising various asynchronous busses or serial data streams. In this embodiment, the random data arrives at a data bus output as a data output signal, and is fed back to a comparator device that compares the data output signal with the original random number. The comparator implements logic for comparing the random data received from the CORE to the random data that was sent into the core. If the data is correct, the output of the comparator circuit will generate signals for enabling the clock frequency provided by clock generator circuit 30 to be increased in a manner so as to achieve a maximum value that avoids a failure point.

[0014] In each embodiment, once the IC chip is in a free running state, the monitoring of data will continue to ensure that the errors do not occur as the chip incurs different operating conditions. The clock rate will be accordingly adjusted.

[0015] Particularly, the clock frequency may be adjusted at a clock supply circuit in a central location and the clock would then be distributed to the source and receive logic. The clock could be sourced by a PLL or a simple oscillator and the frequency adjusted during operation using the error rate detection circuitry to increase or decrease the clock frequency. Frequency adjustment may be implemented with circuitry that changes PLL control signals or, simply by circuitry that divides the clock until the desired level of data integrity is reached. Timing of the source and receive logic can be analyzed in a best-case scenario since the clock frequency will be automatically adjusted to compensate for manufacturing process conditions and operating parameters during operation.

Brief Description of the Several Views of the Drawings

[0016]

Further features, aspects and advantages of the apparatus and methods of the

present invention will become better understood with regard to the following description, appended claims, and the accompanying drawings where:

[0017] Figure 1 is a block diagram illustrating the novel clock signal adjustment circuit implementing Error Correcting Code check according to a first embodiment of the invention.

[0018] Figure 2 is a block diagram illustrating the novel clock signal adjustment circuit implementing implementing data error checking according to a second embodiment of the invention.

[0019] Figure 3 is a block diagram illustrating the novel clock signal adjustment circuit implementing random number generator and IC processing according to a third embodiment of the invention.

Detailed Description of the Invention

[0020] Detailed Description of the Preferred Embodiments

[0021] Figure 1 is a block diagram depicting the novel error correcting system architecture 10 according to a first embodiment of the invention. As shown in Figure 1, there is provided a source circuit device 12 for transmitting data signals through ECC error correction circuitry 20 to a destination device such as IC receiver device 15 according to clock timing signals 18 provided by clock generator circuit 30. As shown in Figure 1, the source transmitter circuit 12 is coupled to an error correcting code (ECC) generator circuit device 20 that generates ECC bits in accordance with the data that is received from the transmitter 12. The ECC generator 20 receives data from the transmitter 12 and, outputs the data plus error correction information according to known techniques. Coupled to the ECC generator device 20 is a novel error correcting code (ECC) check circuit device 25 which, in turn, is coupled to a destination receiver device 15 for receiving the transmitted data. As will be described in further detail herein, ECC generate 20 and ECC check 25 devices ensure the integrity of real data 19 communicated between respective transmit source and destination receive circuits 12, 15 within the IC. As shown in Figure 1, the system architecture 10 is provided with an input reset signal 28 which when activated, triggers a system learning cycle for initializing clock timing signals so that data transmission rates may be optimized

according to the characteristics of the IC.

[0022] Specifically, at reset, a learning cycle is implemented where a series of predefined transmissions or, a pseudo random bit stream, is generated from the transmit source 12. Along with the transmitted data, an error code is generated by ECC generator circuit 20 which may include simple parity to other forms of error correction, e.g., convolution (tree) or block codes. Particularly, the transmitted data and ECC error code is input to a complementary ECC check circuit 25 that determines the error check rate, e.g., how many bit errors occur in a unit of time. This error check rate is input to a monitor device 28 which functions to compare the rate of error correction against an acceptable margin. The output of the monitor device 28 is then fedback as a signal 32 to adjust the clock rate 18 for the IC and, consequently, the ECC error correction rate, until an acceptable rate of error correction is achieved. It should be understood that the error correcting system architecture 10 according to a first embodiment of the invention is used to optimize the timing clock signal 18 in real time.

[0023] Figure 2 is a block diagram depicting the novel error correcting system architecture 30 according to a second embodiment of the invention. As shown in Figure 2, the transmitter, receiver and clock generator circuits are identical to the like elements depicted in Figure 1, however, there is included a novel error check error check circuit 33 that checks for errors in real time. At reset, a learning cycle is implemented where a series of predefined error code transmissions or, a pseudo random bit streams, are generated from the transmit source 12 destined for error check circuit 33 over error codes lines 55. It is understood that the error code lines may comprise a single conductor or even a data bus. In accordance with this second embodiment, implementing wiring tools during the final production development phase, i.e., "PD" cycles, the load on the error codes lines 55 is fixed in such a way to provide a signal delay, as compared to data traveling over data line 19 directly from the transmitter 12 to the receiver 15. In one embodiment, the delay may be accomplished with capacitive loading, for instance of conductors 55.

[0024] Preferably, according to the second embodiment, at reset, a learning cycle is implemented where a series of predefined transmissions is generated from the

transmit source 12. According to the invention, during the test time, the error check circuitry 33 (Figure 2) will monitor to a first fail point, and then pick a clock tap of sufficient guard band to guarantee the error free arrival of the data. That is, as the error check circuit 30 is informed of the bit signal patterns output from the transmitter, it knows what signals to expect at each iteration. Thus, during the learning cycle, for each one or a series of outputs generated from the transmit source 12, the clock signal 18 is gradually increased, for example. Thus, the generated signal patterns along line 55 are sufficiently delayed so that they may be read by the error checker circuit 33. As the clock signal 18 input to the transmitter effects the timing of signals generated at the transmit source 12, the error check circuit will monitor the delayed transmitter output, and verify whether the correct data signal patterns were correctly received. As soon as a failure is detected or a failure rate that exceeds a minimum threshold is detected at the error check circuit 33, indicating an excessive clock speed 18, a signal 32 may be fed back to the clock generator circuit 30 in order to decrease the clock speed. The clock speed may be adjusted until no failures are detected at the error check circuit, or at least until failures are detected below a certain failure rate. It should be understood that, in order to insure that the error correction wires are slower than the rest of the bus, the wiring tool may introduce deliberate delay though the use of additional delay buffers and capacitance on the wires forming the error correction lines 55 which would cause the error bits to be the first to fail. The data path would still be intact and allow the data to still be transmitted while the clock generation circuit is being slowed down. In order to implement this setup, the error correction code requires it's own error correction to be able to identify that the ECC signals were the ones that were failing.

[0025] Preferably, after the reset cycle, once the chip is in a free running state, the error lines 55 may continue to be monitored by error correction circuit 33 to ensure that the errors do not occur as the chip incurs different operating conditions and, the clock rate is accordingly adjusted.

[0026] Particularly, as shown in Figures 1 and 2, the clock frequency of the link may be adjusted at the clock supply circuit 30 which may be centrally located, and the clock signal 18 is then distributed to the source and destination receive logic circuits. The clock may be sourced by a PLL or a simple oscillator (not shown) and the frequency

adjusted during operation using the error rate detection circuitry to increase or decrease the clock frequency. Frequency adjustment may be implemented with circuitry that changes PLL control signals or, simply by dividing the clock signal by suitable circuitry until the desired level of data integrity is reached. Timing of the source and receive logic can be analyzed in a best-case scenario since the clock frequency will be automatically adjusted to compensate for manufacturing process conditions and operating parameters during operation.

[0027] More specifically, as shown in Figures 1 – 2, the ECC check and error correction circuits, while in reset mode, sends a comparison output logic signal 32 back to the originating clock source 30. This logic signal 32 is fed back to the clock generator circuit 30 along two lines to indicate that the clock frequency needs to be changed. For example, one line may indicate that a clock frequency change is needed, while the second line may indicate that a clock frequency increase "1" or decrease "0" is needed. This feedback 32 is input to the clock generation circuitry 30 which accordingly switches to the new clock frequency. A new set of test data may subsequently be sent out to attempt to establish if the clock rate was correct.

[0028] According to a third embodiment, shown in Figure 3, there is depicted a detailed dataflow diagram of the error generation and correction circuitry 75. In this embodiment, at system reset, the current value of the Real Time Clock (RTC) 35 is input to an optimizer circuit 39 comprising a SEED register 40 which seeds a random number generator 45. In one embodiment, a SEED is initialized, and then incremented every clock cycle. With this SEED, a unique random number 56 is generated with any pseudo-random, linearly distributed algorithm known to skilled artisans (such as XORing the bits with themselves). This unique random number 56 is transmitted throughout a data path of a semiconductor circuit, e.g., a "system on chip", also referred to as a CORE circuit 60 comprising the IC, in Figure 3.

[0029]

Particularly, this random data 56 is fed to the start of the dataflow path 56a at the input of the CORE circuit 60 and the data is transmitted through various asynchronous busses or serial data streams. In one embodiment depicted in Figure 3, processing flow through the CORE circuit 60 includes devices such as data busses 57a, 57b and various logic block/bridges 58a, 58b to the output. Finally, the random data arrives at

a data bus output 57b as data output signal 65, and is returned back to the comparator device 70 provided in the optimizer 39. In the optimizer 39, the original random data 56 is input to the error detecting comparator device 70 implementing logic for comparing the random data 65 received from the CORE 60 to the random data 56 that was sent into the core 60. If the data is correct, the output of the comparator circuit 70 will generate signals 32 for enabling the clock frequency provided by clock generator circuit 30 to be increased. That is, if the system on chip (SOC) is operating at an operable frequency and no data errors occur, then the data 65 received will match the data 56 that what was sent and the clock frequency may be increased. If the data does not match, then the system clock 30 is running too fast and the frequency must be decreased. That is, if any errors are found as a result of the comparison, the clock taps 34 provided in clock generator circuit 30 may be increased to step down the clock frequency. Thus, as shown in Figure 3, the frequency of clock signal 30 is chosen from several clock taps via a multiplexor 72.

[0030] In the preferred embodiment, the entire processes depicted in Figures 1-3 is repeated frequently with a new set of test data in an attempt to establish if the clock rate is correct. The processes depicted in Figures 1-3 may additionally be repeated during normal device operation to ensure that the errors do not occur as the chip incurs different operating conditions.

[0031] While the invention has been particularly shown and described with respect to illustrative and preformed embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention which should be limited only by the scope of the appended claims.